IN THE CLAIMS

Please cancel claims 14 and 24-27 without prejudice or disclaimer.

Please amend claims 1, 12 and 16 as indicated below.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended) A method of producing an integrated circuit (IC) device layout representation corresponding to an IC device design, said method comprising:

(a) generating an initial layout representation in accordance with a plurality of design rules;

(b) simulating how structures within at least a portion of the initial layout representation will pattern on a wafer;

(c) based on the simulating step, identifying portions of the layout representation which include structures demonstrating poor manufacturability;

(d) based on the simulating step, identifying portions of the layout representation in which extra manufacturability margin is present; and

(e) modifying at least one of (i) portions of the layout representation which include structures demonstrating poor manufacturability and (ii) portions of the layout representation in which extra manufacturability margin is present;

wherein for portions of the layout representation including structures demonstrating poor manufacturability, step (e) includes:

at least one of (i) providing more space between adjacent structures, (ii) decreasing linewidth of one or more structures, and (iii) making edges of one or more structures wider.

Claim 2 (original) The method of claim 1, said method further comprising:

(f) simulating how structures within at least a portion of the modified layout representation will pattern on a wafer; and

(g) repeating steps (c) – (f) until no portions of the layout representation demonstrate poor manufacturability.

Claim 3 (original) The method of claim 1, said method further comprising:

performing at least one optical proximity correction (OPC) on the initial layout representation before step (b).

Claim 4 (original) The method of claim 1, wherein step (c) includes:

performing optical rule checking (ORC) on the simulated layout representation.

Claim 5 (original) The method of claim 4, wherein performing ORC includes checking at least one of aerial image metrics, resist image metrics and post exposure bake metrics.

Claim 6 (original) The method of claim 5, wherein ORC is performed on one or more portions of the simulated layout representation over a process window of focus and intensity.

Claim 7 (original) The method of claim 5, wherein the aerial image metrics include at least one of image edge slope, image edge log slope, contrast, minimum intensity, maximum intensity, edge placement error and intensity at a given distance.

Claim 8 (original) The method of claim 1, wherein step (c) includes:

defining a manufacturability figure of merit (FOM); and

evaluating the manufacturability of at least a portion of the simulated layout representation based on the manufacturability FOM.

Claim 9 (original) The method of claim 8, wherein defining a manufacturability FOM includes:

identifying one or more metrics which are indicative of a manufacturable layout representation; and

selecting acceptable ranges for the one or more metrics.

Claim 10 (original) The method of claim 9, wherein the evaluating step includes:

performing optical rule checking (ORC) on the simulated layout representation using the selected acceptable ranges for the one or more metrics.

Claim 11 (original) The method of claim 10, wherein the one or more metrics include at least one of image edge slope, image edge log slope, contrast, minimum intensity, maximum intensity, edge placement error and intensity at a given distance.

Claim 12 (currently amended) ~~The method of claim 9, wherein defining a manufacturability FOM includes:~~ A method of producing an integrated circuit (IC) device layout representation corresponding to an IC device design, said method comprising:

(a) generating an initial layout representation in accordance with a plurality of design rules;

(b) simulating how structures within at least a portion of the initial layout representation will pattern on a wafer;

(c) based on the simulating step, identifying portions of the layout representation which include structures demonstrating poor manufacturability;

(d) based on the simulating step, identifying portions of the layout representation in which extra manufacturability margin is present; and

(e) modifying at least one of (i) portions of the layout representation which include structures demonstrating poor manufacturability and (ii) portions of the layout representation in which extra manufacturability margin is present;

wherein step (c) includes:

defining a manufacturability figure of merit (FOM); and

evaluating the manufacturability of at least a portion of the simulated layout representation based on the manufacturability FOM;

wherein defining a manufacturability FOM includes:

identifying one or more metrics which are indicative of a manufacturable layout representation;

selecting acceptable ranges for the one or more metrics;

selecting an exemplary layout;

generating a simulation image corresponding to how the selected exemplary layout pattern will pattern on a wafer;

evaluating a scanning electron microscope (SEM) image of the selected exemplary layout portion printed on a wafer;

identifying areas on the SEM image that are problematic with respect to manufacturability; and

for each problematic area on the SEM image, locating the corresponding portion of the simulation image and determining acceptable ranges for the one or more metrics based on the simulation image.

Claim 13 (original) The method of claim 1, wherein step (c) includes:

identifying metrics which are indicative of a manufacturable layout representation.

Claim 14 (cancelled)

Claim 15 (original) The method of claim 1, wherein for portions of the layout representation in which extra manufacturability margin is present, step (e) includes:

compacting at least a portion of the layout representation.

Claim 16 (currently amended) ~~The method of claim 1,~~ A method of producing an integrated circuit (IC) device layout representation corresponding to an IC device design, said method comprising:

(a) generating an initial layout representation in accordance with a plurality of design rules;

(b) simulating how structures within at least a portion of the initial layout representation will pattern on a wafer;

(c) based on the simulating step, identifying portions of the layout representation which include structures demonstrating poor manufacturability;

(d) based on the simulating step, identifying portions of the layout representation in which extra manufacturability margin is present; and

(e) modifying at least one of (i) portions of the layout representation which include structures demonstrating poor manufacturability and (ii) portions of the layout representation in which extra manufacturability margin is present;

wherein for portions of the layout representation in which extra manufacturability margin is present, step (e) includes:

at least one of (i) moving outer corners of structures closer to adjacent structures, (ii) moving contacts closer to inner corners of metal lines, (iii) moving contacts closer to polysilicon end caps, (iv) reshaping active or metal layers to maintain width and space, and (v) adding side extensions to polysilicon end caps.

Claim 17 (original) The method of claim 1, wherein step (b) includes simulating how structures will pattern on a wafer as a result of at least one of resolution enhancement technologies (RET), optical proximity correction (OPC), proximity to other structures, density of structures and corner rounding.

Claim 18 (original) The method of claim 1, wherein step (e) includes violating at least one of the plurality of design rules.

Claim 19 (original) The method of claim 1, wherein step (e) is performed despite there existing no violation of any of the plurality of design rules.

Claim 20 (original) The method of claim 1, wherein step (c) includes providing a graphical representation indicating structures demonstrating poor manufacturability.

Claim 21 (original) The method of claim 20, wherein step (d) includes providing a graphical representation identifying portions of the layout representation in which extra manufacturability margin is present.

Claims 22-27 (cancelled)